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APPLICATION FOR LETTERS PATENT

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Methods Of Forming Capacitors, Methods Of Forming
Capacitor-Over-Bit Line Memory Circuitry, And
Related Integrated Circuitry Constructions

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1 **METHODS OF FORMING CAPACITORS, AND METHODS OF**
2 **FORMING CAPACITOR-OVER-BIT LINE MEMORY CIRCUITRY, AND**
3 **RELATED INTEGRATED CIRCUITRY CONSTRUCTIONS**

4 **TECHNICAL FIELD**

5 This invention relates to methods of forming capacitors, to methods
6 of forming capacitor-over-bit line memory circuitry, and to related
7 integrated circuitry constructions.

8 **BACKGROUND OF THE INVENTION**

9 As integrated circuitry continues to shrink in size, efforts are
10 ongoing to find novel methods of forming integrated circuitry structures
11 and related integrated circuitry which improve upon those methods
12 currently utilized and the resultant structures formed thereby.

13 One type of integrated circuitry is memory circuitry. Such circuitry
14 has been and continues to be the focus of intense efforts to reduce the
15 size of the circuitry, increase the speed with which such circuitry
16 operates, and maintain or increase the ability of such circuitry to
17 perform its memory function.

18 Accordingly, this invention arose out of concerns associated with
19 improving the methods by which integrated circuitry, and in particular,
20 integrated memory circuitry is formed. This invention also arose out of
21 concerns associated with providing improved integrated circuitry
22 constructions.
23

SUMMARY OF THE INVENTION

Methods of forming capacitors, methods of forming capacitor-over-bit line memory circuitry, and related integrated circuitry constructions are described. In one embodiment, a capacitor storage node is formed having an uppermost surface and an overlying insulative material over the uppermost surface. Subsequently, a capacitor dielectric functioning region is formed discrete from the overlying insulative material operably proximate at least a portion of the capacitor storage node. A cell electrode layer is formed over the capacitor dielectric functioning region and the overlying insulative material. In another embodiment, a capacitor storage node is formed having an uppermost surface and a side surface joined therewith. A protective cap is formed over the uppermost surface and a capacitor dielectric layer is formed over the side surface and protective cap. A cell electrode layer is formed over the side surface of the capacitor storage node. In yet another embodiment, a plurality of capacitor storage nodes are formed arranged in columns. A common cell electrode layer is formed over the plurality of capacitor storage nodes. Cell electrode layer material is removed from between the columns and isolates individual cell electrodes over individual respective capacitor storage nodes. After the removing of the cell electrode layer material, conductive material is formed over portions of remaining cell electrode material thereby placing some of the individual cell electrodes into electrical communication with one another.

BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic side sectional view of a semiconductor wafer fragment in process in accordance with one embodiment of the present invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 4.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 5.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 7.

Fig. 9 is a view of the Fig. 1 wafer fragment at a processing step which is subsequent to that which is shown in Fig. 8.

1 Fig. 10 is a view of the Fig. 1 wafer fragment at a processing
2 step which is subsequent to that which is shown in Fig. 9.

3 Fig. 11 is a view of the Fig. 1 wafer fragment at a processing
4 step which is subsequent to that which is shown in Fig. 10.

5 Fig. 12 is a view taken along line 12-12 in Fig. 11.

6 Fig. 13 is a schematic circuit diagram of electronic circuitry formed
7 in accordance with the inventive methodologies.

8 9 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

10 This disclosure of the invention is submitted in furtherance of the
11 constitutional purposes of the U.S. Patent Laws "to promote the progress
12 of science and useful arts" (Article 1, Section 8).

13 Referring to Fig. 1, a semiconductor wafer fragment in process is
14 shown generally at 20 and comprises semiconductive substrate 22. In the
15 context of this document, the term "semiconductive substrate" is defined
16 to mean any construction comprising semiconductive material, including,
17 but not limited to, bulk semiconductive materials such as a
18 semiconductive wafer (either alone or in assemblies comprising other
19 materials thereon), and semiconductive material layers (either alone or
20 in assemblies comprising other materials). The term "substrate" refers
21 to any supporting structure, including, but not limited to, the
22 semiconductive substrates described above.

1 Conductive lines 24, 26, 28, and 30 are formed over substrate 22
2 and include a gate oxide layer (not specifically shown), a conductive
3 polysilicon layer 32, a silicide layer 34, an insulative cap 36, and sidewall
4 spacers 38. Other conductive line constructions can, of course, be used.
5 Shallow isolation trenches 40 are provided and are backfilled with
6 dielectric material and are planarized. Isolation regions 40 can also be
7 provided through other techniques such as field oxide isolation
8 techniques. Diffusion regions 42, 44, and 46 are formed within substrate
9 22 intermediate respective conductive lines. The diffusion regions
10 typically comprise regions of the substrate which are implanted with
11 suitable impurities.

12 Referring to Fig. 2, a buried digit line 47 is formed and is
13 encapsulated in an insulative layer such as borophosphosilicate glass
14 (BPSG) 48 that is formed over substrate 22. Openings 50, 52 are
15 formed in the insulative layer 48. The openings are formed over and
16 join with respective diffusion regions 42, 46. Conductive material 54,
17 e.g. conductively doped polysilicon, is formed over the substrate and
18 within opening 50, 52. The buried digit line 47 is shown as a dashed
19 line to emphasize that the buried digit line does not connect to (e.g.,
20 is behind, or is below the plane of Fig. 2) the conductive material 54
21 formed in the openings 50 and 52. Conductive material 54 can be
22 subsequently planarized for isolation purposes. Conductive material 54
23 establishes electrical communication with the respective diffusion regions

1 over which it is formed and will provide electrical communication
2 between capacitor storage nodes which are to be formed as described
3 below.

4 Referring to Fig. 3, a layer of material 56 is formed over
5 substrate 22 and has a generally planar outer surface 58. For purposes
6 of the ongoing discussion, layer 56 comprises a first insulative layer of
7 material. An exemplary material is BPSG.

8 Referring to Fig. 4, a plurality of openings are formed over or
9 within layer 56, with exemplary openings being shown at 60, 62. In the
10 illustrated and preferred embodiment, opening 60, 62 are formed to
11 expose uppermost portions of conductive material 54.

12 Referring to Fig. 5, conductive material 64 is formed over
13 substrate 22 and received within openings 60, 62. In the illustrated
14 example, conductive material 64 is formed sufficiently to overfill the
15 openings. It is possible, however, to only partially fill or underfill the
16 openings for purposes which will become apparent below.

17 Referring to Fig. 6, portions of conductive material 64 are
18 removed, as by planarization or other methods, to electrically isolate the
19 conductive material within the openings formed within and laterally
20 adjacent insulative layer 56. Such forms, in one embodiment, a plurality
21 of capacitor storage nodes. Exemplary storage nodes are shown
22 at 66, 68. The storage nodes, as formed, are arranged in columns which
23 are disposed into and out of the plane of the page upon which Fig. 6

1 appears. Specifically, in this example storage node 66 constitutes one
2 of a plurality of storage nodes arranged in one column which extends
3 into and out of the plane of the page; and, storage node 68 constitutes
4 one of a plurality of storage nodes in a different column which extends
5 into and out of the plane of the page. Each column constitutes an
6 array of storage nodes. The storage nodes can also be formed as
7 containers or cup-like structures, with subsequent processing taking place
8 substantially as described below.

9 Referring to Fig. 7, portions of conductive material 64 are
10 removed sufficiently to less than fill each opening 66, 68 respectively.
11 Accordingly, such constitutes but one way in which each opening can be
12 less than filled with conductive material. It is possible, as mentioned
13 above, for each opening to be less than filled with conductive material
14 by other techniques. For example, a conformal deposition of conductive
15 material, e.g. polysilicon, can be conducted to less than fill the openings.

16 In this example, overfilled portions of conductive material 64 are
17 removed to below outer surface 58 of first insulative material layer 56,
18 thereby partially filling each respective opening. Accordingly, each
19 storage node received within layer 56 has an upper surface 66a, 68a
20 respectively, which is disposed elevationally below outer surface 58. The
21 illustrated upper surfaces 66a, 68a constitute uppermost surfaces, and
22 each storage node has a side surface 66b, 68b respectively joined with
23 its associated uppermost surface.

1 Referring to Fig. 8, an overlying insulative material 70 is formed
2 over the uppermost surfaces 66a, 68b of respective storage nodes 66, 68.
3 In the illustrated example, the formation of insulative material 70
4 constitutes filling remaining opening portions with insulative material.
5 Insulative material 70 is preferably different from material comprising
6 layer 56 for reasons which will become apparent below. An exemplary
7 material is an oxide formed through decomposition of TEOS. In this
8 example and for purposes of the ongoing discussion, insulative material
9 70 comprises a second different insulative layer of material, at least a
10 portion of which is disposed within remaining opening portions. Such
11 material can be formed by overfilling the remaining opening portions and
12 planarizing the material relative to outer surface 58 of layer 56.
13 Alternately by way of example only, the layer can be etched back
14 through a timed etch.

15 In one embodiment, a sufficient amount of insulative material is
16 formed over each storage node such that an insulative material
17 surface 70a is generally coplanar with generally planar outer surface 58.

18 Alternately considered, protective caps 72 are formed over
19 uppermost surfaces 66a, 68a, with each cap being formed within at least
20 a remaining portion of each opening. The protective caps are insulative
21 in nature and formed over, and in this example, not laterally proximate
22 conductive material comprising each storage node.
23

1 Referring to Fig. 9, portions of first insulative material layer 56
2 are removed to expose portions of side surfaces 66b, 68b respectively.
3 In one embodiment, material of layer 56 is etched selectively relative to
4 insulative material 70. Such constitutes removing material which is
5 laterally adjacent each storage node sufficiently to expose respective side
6 portions thereof. In this example, storage node portions are partially
7 exposed by the removal of material of layer 56. Accordingly, side
8 surfaces 66b, 68b have respective first portions (undesigned) which are
9 disposed elevationally higher than an adjacent insulative material upper
10 surface 74, and respective second portions (undesigned) which are
11 disposed elevationally lower than the adjacent insulative material upper
12 surface 74. In another embodiment, the removal of material of layer 56
13 comprises etching such material faster than any of second insulative
14 material 70 sufficiently to expose portions of each capacitor node.

15 Referring to Fig. 10, a layer of roughened polysilicon 76, e.g.
16 hemispherical grain (HSG) polysilicon or cylindrical grain polysilicon, is
17 formed over exposed portions of each storage node. A capacitor
18 dielectric layer 78 is formed over the exposed side surfaces of each
19 storage node and corresponding portions of each node's protective
20 cap 72. Such forms capacitor dielectric functioning regions which are
21 discrete from the overlying insulative material 70 operably proximate at
22 least a portion of the capacitor storage node.

1 A common cell electrode layer 80 is formed over capacitor
2 dielectric layer 78, insulative material 70, and the previously-exposed side
3 surfaces of the storage nodes. In this example, layer 80 is formed
4 laterally proximate the respective side surface first portions which were
5 previously exposed. Alternately considered, the array of storage nodes
6 is first electrically interconnected in a capacitor array configuration with
7 common cell electrode layer 80.

8 Referring to Fig. 11, a number of processing steps have taken
9 place. First, material of common cell electrode layer 80 has been
10 removed from between the columns defined by each of the respective
11 storage nodes. Common cell electrode layer material is also preferably
12 removed from over the individual protective caps. In one embodiment,
13 cell electrode material is left only over generally vertical surfaces. Such
14 serves to isolate individual cell electrodes over their respective capacitor
15 storage nodes. In one embodiment, the removal of material of the
16 common cell electrode layer 80 comprises anisotropically etching such
17 layer and forming individual bands or rings 82, 84 around the node
18 portions which were previously exposed. Overlying insulative layer 70
19 provides protection during the removal of the material of cell electrode
20 layer 80 so that the risk of exposure and removal of layer 78 adjacent
21 polysilicon 76 can be greatly reduced if not eliminated. In turn,
22 subsequent risks of shorting between the cell plate and storage node can
23 be greatly reduced if not eliminated. In a preferred embodiment, such

1 bands are also formed over portions of the protective caps as shown.
2 In a preferred embodiment, such is accomplished through a maskless
3 etch. In the context of this document, the term "maskless" will be
4 understood to only mean no masking of the area of the layer being
5 etched for purposes of isolating the layer, without requiring no masking
6 of the layer elsewhere on the substrate.

7 A third insulative material 86 is formed over the substrate including the
8 isolated cell electrodes or bands 82, 84. An exemplary material is
9 BPSG. Such material is formed over remaining cell electrode material.
10 Openings 88 are patterned and etched into layer 86, and preferably
11 expose at least some of the remaining cell electrode material or rings
12 82, 84. Conductive material 90, e.g. conductively doped polysilicon, is
13 formed within openings 88 and preferably electrically interconnects at
14 least some of the isolated individual cell electrodes. Material 90 can be
15 planarized to have a generally planar upper surface which is coplanar
16 with the upper surface of material 86.

17 Alternately considered, formation of openings 88 constitutes etching
18 a plurality of trenches into the third insulative material and exposing
19 isolated individual cell electrodes. Subsequently, conductive material 90
20 is formed over the substrate and fills the trenches. Such constitutes
21 second electrically interconnecting some of the isolated cell electrodes
22 with conductive material. By "second electrically interconnecting" is
23 meant that initially, when the cell electrode layer is blanket deposited

1 over the substrate, the cell electrodes for the individual storage
2 capacitors can be considered as being first electrically interconnected.
3 When the conductive material of the cell electrode layer is removed
4 from between the columns of arranged storage capacitors, such can be
5 considered as electrically disconnecting the cell electrodes for the
6 individual storage capacitors. Hence, when conductive material 90 is
7 formed over the selected, isolated cell electrode material, such can be
8 considered as electrically interconnecting some of the cell electrode
9 material for a second time thereby placing them into electrical
10 communication with one another.

11 Conductive material 92 is subsequently formed over the substrate
12 and patterned into conductive lines which extend to outside circuitry.
13 *Exemplary outside circuitry includes sensing circuitry.*

14 Referring to Figs. 11 and 12, integrated circuitry is provided. In
15 one embodiment, a capacitor storage node is provided and includes an
16 uppermost surface 66a and a side surface 66b joined therewith. A
17 protective cap 70 is provided over uppermost surface 66a, and a
18 capacitor dielectric layer 78 is disposed over side surface 66b. A cell
19 electrode band 82 is disposed proximate at least a portion of storage
20 node side surface 66b, and not over storage node uppermost surface 66a.
21 Protective cap 70 has a side surface (not specifically designated), and in
22 one embodiment, cell electrode band 82 is disposed laterally proximate
23 at least a portion of the protective cap side surface. In another

1 embodiment, cell electrode band 82 is disposed over less than an entirety
2 of storage node side surface 66b. In yet another embodiment, cell
3 electrode band 82 has an uppermost portion which extends elevationally
4 higher than any material of capacitor storage node 66.

5 In another embodiment, integrated circuitry includes a capacitor
6 storage node 66 having an uppermost surface 66a. An insulative
7 material 70 overlies uppermost surface 66a. A capacitor dielectric
8 functioning region which is discrete from overlying insulative material 70
9 is disposed operably proximate at least a portion of the capacitor storage
10 node. A cell electrode layer 82 is disposed laterally proximate the
11 capacitor dielectric functioning region and overlying insulative material
12 70. In one embodiment, a substantial portion of the dielectric
13 functioning region is disposed only laterally proximate the capacitor
14 storage node. In another embodiment, the dielectric functioning region
15 comprises a layer of dielectric material 78 which extends over overlying
16 insulative material 70 and defines a non-dielectric functioning region.
17 In another embodiment, the dielectric functioning region defines a band
18 of dielectric material (Fig. 12) which laterally encircles at least a portion
19 of storage node 66. In yet another embodiment, cell electrode layer 82
20 defines a band of conductive material which laterally encircles at least
21 a portion of storage node 66. In yet another embodiment, cell electrode
22 layer 82 comprises an uppermost band portion which extends elevationally
23 higher than storage node uppermost surface 66a.

1 In another embodiment, a capacitor-over-bit line memory array is
2 provided and includes a substrate 22 having a pair of spaced-apart
3 conductive lines 26, 28 disposed thereover. A pair of diffusion
4 regions 42, 46 are received within substrate 22 operably proximate
5 conductive lines 26, 28. Conductive material 54 is disposed over and in
6 electrical communication with diffusion regions 26, 28 respectively, and
7 extends away therefrom. A pair of capacitor storage nodes 66, 68 are
8 provided, each of which is operably joined with and in electrical
9 communication with a respective one of the diffusion regions through the
10 conductive material disposed thereover. Each storage node has an
11 uppermost surface 66a, 68a respectively, and a respective side
12 surface 66b, 68b joined therewith. A protective cap 70 is provided over
13 each uppermost surface 66a, 68a, and a capacitor dielectric layer 78 is
14 disposed over each side surface 66b, 68b. Cell electrode bands 82, 84
15 are respectively disposed proximate at least a portion of each associated
16 storage node side surface 66b, 68b respectively, and not over the
17 associated storage node uppermost surface 66a, 68a. The capacitor-over-
18 bit line circuitry just described can have any of the constructions
19 discussed above.

20 Referring to Fig. 13, a circuit schematic is shown which depicts a
21 DRAM cell having an access transistor, a bit line BL, a storage
22 capacitor C, and a segmented field plate column line PL. In a
23 preferred embodiment, the segmented field plate column line PL is

1 defined by either or both of conductive materials 90, 92 (Fig. 11).
2 Whereas in the past, the field plate or cell electrode was shared by all
3 of the capacitors in the memory array of a DRAM, the present
4 invention provides methods by which discrete columns of capacitors can
5 be connected into columns which can be selectively used, individually and
6 directly in sensing applications.

7 Advantages can also be achieved in improving the voltage swing
8 across the capacitors in the memory array and in improving the
9 differential voltage signal as compared with the differential signal
10 produced by an array having a common shared cell plate layer. Other
11 advantages will be apparent to the skilled artisan.

12 In compliance with the statute, the invention has been described
13 in language more or less specific as to structural and methodical
14 features. It is to be understood, however, that the invention is not
15 limited to the specific features shown and described, since the means
16 herein disclosed comprise preferred forms of putting the invention into
17 effect. The invention is, therefore, claimed in any of its forms or
18 modifications within the proper scope of the appended claims
19 appropriately interpreted in accordance with the doctrine of equivalents.
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